

Kasarani Campus Off Thika Road Tel. 2042692 / 3 P. O. Box 49274, 00100 NAIROBI Westlands Campus Pamstech House Woodvale Grove Tel. 4442212

KIRIRI WOMENS' UNIVERSITY OF SCIENCE AND TECHNOLOGY UNIVERSITY EXAMINATION, 2016/2017 ACADEMIC YEAR FIRST YEAR, SECOND SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE (COMPUTER SCIENCE)

Date: 16th August, 2016. Time: 11.00am – 1.00pm

Fax: 4444175

KCS 103 - INTRODUCTION TO COMPUTER ORGANIZATION

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTION ONE (COMPULSORY) AND ANY OTHER TWO QUESTIONS

QUESTION ONE (30 MARKS)

a) Define an instruction set and explain four functions of a complete instruction set.

(6 Marks)

b) Distinguish between computer architecture and organization and provide relevant examples.

(6 Marks)

- c) Evaluate the following expressions, giving the answer in hexadecimal.
 - i) $2170_8 + 1C3_{16}$
 - ii) $3AE_H + 7253_8$

(6 Marks)

d) Using two's complement, compute -25₁₀-39₁₀.

(4 Marks)

c) Using an appropriate Von Neumann diagram, explain how the CPU performs the addition of two numbers.

(8 Marks)

QUESTION TWO (20 MARKS)

a) Describe the assembly language syntax.

(6 Marks)

- b) Distinguish the following;
 - i) Write through and write back system.

(4 Marks)

ii) Memory Address Register and Memory Buffer Register.

(4 Marks)

c)	An instruction cycle is the basic operation cycle of a computer. Using a wel explain the concept of the Instruction cycle.	l labeled diagram,	
		(6 Marks)	
<u>QUE</u>	ESTION THREE (20 MARKS)		
a)	Discuss four differences between SRAM and DRAM.		
b)	Explain five differences between CISC and RISC computing.	(4 Marks)	
c)	Distinguish unified cache and split cache, stating their effect on miss ratio and ba	(10 Marks) andwidth. (6 Marks)	
<u>QUE</u>	ESTION FOUR (20 MARKS)	(o mas)	
a)	Explain any three principles of Von Neumann architecture .	(2 Moulto)	
b)	Describe four types of Read Only Memories (ROMS)	(3 Marks)	
c)	Acache is used by the central processing unit (CPU) of a computer to reduce to access <i>memory</i> . Describe three common organizations for cache placement.	(4 Marks) d by the central processing unit (CPU) of a computer to reduce the average time to V Describe three common organizations for cache placement	
1\	·	(6 Marks)	
d)	Describe the fields of the Processor Status Word (PSW) register	(7 Marks)	
<u>QUF</u>	ESTION FIVE (20 MARKS)		
a)	Describe three basic input/ output techniques.		
b)	With the aid of a diagram, explain the Central processing unit (CPU) pins.	(6 Marks)	
c)	Explain three goals of computer hierarchy.	(8 Marks)	

Describe three categories of I/O devices

d)

to

(3 Marks)

(3 Marks)