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KIRIRI WOMENS' UNIVERSITY OF SCIENCE AND TECHNOLOGY
UNIVERSITY EXAMINATIONS, 2019/2020 ACADEMIC YEAR
THIRD YEAR, FIRST SEMESTER EXAMINATIONS
FOR THE BACHELOR OF SCIENCE
(COMPUTER SCIENCE)

Date: 15th April 2019
Time: 11.00 – 1pm

KCS 304 – COMPUTER ARCHITECTURE

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTION ONE (COMPULSORY) AND ANY OTHER TWO QUESTIONS

QUESTION ONE (30 MARKS)

a) Define the following terms as used in computers systems;
   i) Cache.
   ii) R.I.S.C.
   iii) C.I.S.C.
   iv) B.I.O.S.
   v) Pipelining.
   vi) Hyper threading.
   vii) Multiprocessing.
   viii) Parallel computing.

(8 Marks)

b) With respect to computer architectures, explain main differences between the Harvard and the Von Neumann architectures of computers.

(3 Marks)

c) Differentiate between the high level and low level programming languages and then give an example in each.

(4 Marks)

d) Discus the main differences between the Compiler and interpreter.

(6 Marks)

e) What is the difference between RAM and Cache?

(2 Marks)

f) A computer system has16 bits data buses, 32 bits address buses, and 8 bit control buses.

i) What is the maximum size of the word can it handle? (2 Marks)

ii) What is the maximum size of RAM the system can address? (3 Marks)

g) In an 8085 microprocessor based system, what will be the contents of registers B and accumulator, after executing the following instructions?

XRA A	Register *A* affected
MVI B, F7$_{Hex}$	Register *B* affected
ADC B	Register *A* affected

(2 Marks)

QUESTION TWO (20 MARKS)

a) Name three types of buses used by computer systems and hence describe their functionalities.

(6 Marks)

b) Describe in details, the Fetch Execute cycle of a microprocessor.
(A timing diagram can be used in describing). (6 Marks)

c) With respect to microprocessor systems explain the purpose/utility of the following registers.

i) Program Counter register.
ii) General purpose register.
iii) Stack Pointerregister.
iv) Instructions register.
v) MAR register.
vi) Temp register.
vii) Flag register.
viii) Accumulator.

(8 Marks)

QUESTION THREE (20 MARKS)

a) State five categories of instructions in Assembly programming language based on the functionality, give an example in each case. (10 Marks)

b) The following are addressing modes for instruction set architecture, used in assembly language programming.

i) Direct Addressing Mode.
ii) Indirect Addressing Mode.
iii) Implicit Addressing Mode.
iv) Register Addressing Mode.
v) Immediate Addressing Mode.

Describe each mode and then give an instruction example for each case. (5 Marks)

c) With reference to ***Intel-8085*** microprocessor and using a suitable flow-chat, write a program to add two numbers stored in the memory locations 2000_{Hex}& 2001_{Hex} respectfully, and then store the result of the operation in the memory location 2010_{Hex}. (5 Marks)
(Refer to the instruction set for Intel 8085 in the last page).

QUESTION FOUR (20MARKS)

a) Computer Memories have undergone various evolutions to develop faster, efficient and high capacities. Describe the types of memories listed below.

i) SRAM.
ii) EPROM.
iii) SDRAM.
iv) EEPROM.
v) DDR-SDRAM.

(5 Marks)

b) Explain five major characteristic differences between the RISC and the CISC microprocessors based on their architecture design and operations. (8 Marks)

c) Using instruction set assemble the program below and hence evaluate the amount of memory in bytes that will be occupied by the assembly program code. (7 Marks)

(Refer to the instruction set for Intel 8085 in the last pages).

	Source program:		
	LXI H, 4000_{Hex}		// Initialize HL index to points 4000H
	MOV A, M		// Get first operand from Memory.
	INX H		// Increment HL index to points 4001H
	SUB M		// Subtract second operand
	INX H		// Increment HL index to 4002H
	MOV M, A		// Store result at 4002H
	HLT		// Terminate program execution

QUESTION FIVE (20MARKS)

a) With respect to Intel 8085 microprocessor, explain the functions of the following assembly instructions.

i) STA4000_h
ii) POP*B*
iii) PUSH*B*
iv) JNC2034_h
v) OUT$F8_h$
vi) DCR*C*
vii) INX*H*
viii) MOV*M, A*

(8 Marks)

b) Outline the main differences between the Microprocessors and Microcontrollers. (4 Marks)

c) Given unlimited memory chips of (4K X 8) and a (2 to 4) decoder chips, design system memory for Intel 8085 based system.Include the data buses, address buses and indicating the memories chips and their memory addresses range. (8 Marks)

INTEL 8085 MICROPROCESSOR INSTRUCTION SET

Hex	mnemonic	Hex	mnemonic	Hex	mnemonic	Hex	mnemonic
CE	ACI 8-Bit	3F	CMC	2B	DCX H	01	LXI B,16-Bit
8F	ADC A	BF	CMP A	3B	DCX SP	11	LXI D,16-Bit
88	ADC B	B8	CMP B	F3	DI	21	LXI H,16-Bit
89	ADC C	B9	CMP C	FB	EI	31	LXI SP,16-Bit
8A	ADC D	BA	CMP D	76	HLT	7F	MOV A A
8B	ADC E	BB	CMP E	DB	IN 8-Bit	78	MOV A B
8C	ADC H	BC	CMP H	3C	INR A	79	MOV A C
8D	ADC L	BD	CMP	04	INR B	7A	MOV A D
8E	ADC M	BE	CMP M	0C	INR C	7B	MOV A E
87	ADD A	D4	CNC 16-Bit	14	INR D	7C	MOV A H
80	ADD B	C4	CNZ 16-Bit	1C	INR E	7D	MOV A L
81	ADD C	F4	CP 16-Bit	24	INR H	7E	MOV A M
82	ADD D	EC	CPE 16-Bit	2C	INR L	47	MOV B A
83	ADD E	FE	CPI 8-Bit	34	INR M	40	MOV B B
84	ADD H	E4	CPO 16-Bit	03	INX B	41	MOV B C
85	ADD L	CC	CZ 16-Bit	13	INX D	42	MOV B D
86	ADD M	27	DAA	23	INX H	43	MOV B E
C6	ADI 8-Bit	09	DAD B	33	INX SP	44	MOV B H
A7	ANA A	19	DAD D	DA	JC 16-Bit	45	MOV B L
A0	ANA B	29	DAD H	FA	JM 16-Bit	46	MOV B M
A1	ANA C	39	DAD SP	C3	JMP 16-Bit	4F	MOV C A
A2	ANA D	3D	DCR A	D2	JNC 16-Bit	48	MOV C B
A3	ANA E	05	DCR B	C2	JNC 16-Bit	49	MOV C C
A4	ANA H	0D	DCR C	F2	JP 16-Bit	4A	MOV C D
A5	ANA L	15	DCR D	EA	JPE 16-Bit	4B	MOV C E
A6	ANA M	1D	DCR E	E2	JPO 16-Bit	4C	MOV C H
E6	ANA 8-Bit	25	DCR H	CA	JZ 16-Bit	4D	MOV C L
CD	CALL 16-Bit	2D	DCR L	3A	LDA 16-Bit	4E	MOV C M
DC	CC 16-Bit	35	DCR M	0A	LDAX B	57	MOV D A
FC	CM 16-Bit	0B	DCX B	1A	LDAX D	50	MOV D B
2F	CMA	1B	DCX D	2A	LHLD 16-Bit	51	MOV D C

Hex	mnemonic	Hex	mnemonic	Hex	mnemonic	Hex	mnemonic
52	MOV D D	71	MOV M C	E5	PUSH H	9E	SBB M
53	MOV D E	72	MOV M D	F5	PUSH PSW	DE	SBI 8-Bit
54	MOV D H	73	MOV M E	17	RAL	22	SHLD 16-Bit
55	MOV D L	74	MOV M H	1F	RAR	30	SIM
56	MOV D M	75	MOV M L	D8	RC	F9	SPHL
5F	MOV E A	3E	MVI A 8-Bit	C9	RET	32	STA 16-Bit
58	MOV E B	06	MVI B 8-Bit	20	RIM	02	STAX B
59	MOV E C	OE	MVI C 8-Bit	07	RLC	12	STAX D
5A	MOV E D	16	MVI D 8-Bit	F8	RM	37	STC
5B	MOV E E	1E	MOV E 8-Bit	D0	RNC	97	SUB A
5C	MOV E H	26	MVI H 8-Bit	C0	RNC	90	SUB B
5D	MOV E L	2E	MVI L 8-Bit	F0	RP	91	SUB C
5E	MOV E M	36	MVI M 8-Bit	E8	RPE	92	SUB D
67	MOV H A	00	NOP	E0	RPO	93	SUB E
60	MOV H B	B7	ORA A	0F	RRC	94	SUB H
61	MOV H C	B0	ORA B	C7	RST 0	95	SUB L
62	MOV H D	B1	ORA C	CF	RST 1	96	SUB M
63	MOV H E	B2	ORA D	D7	RST 2	D6	SUI 16-Bit
64	MOV H H	B3	ORA E	DF	RST 3	EB	XCHG
65	MOV H L	B4	ORA H	E7	RST 4	AF	XRA A
66	MOV H M	B5	ORA L	EF	RST 5	A8	XRA B
6F	MOV L A	B6	ORA M	F7	RST 6	A9	XRA C
68	MOV L B	F6	ORI 8-Bit	FF	RST 7	AA	XRA D
69	MOV L C	D3	OUT 8-Bit	C8	RZ	AB	XRA E
6A	MOV L D	E9	PCHL	9F	SBB A	AC	XRA H
6B	MOV L E	C1	POP B	98	SBB B	AD	XRA L
6C	MOV L H	D1	POP D	99	SBB C	AE	XRA M
6D	MOV L L	E1	POP H	9A	SBB D	EE	XRI 8-Bit
6E	MOV L M	F1	POP PSW	9B	SBB E	E3	XTHL
77	MOV M A	C5	PUSH B	9C	SBB H		
70	MOV M B	D5	PUSH D	9D	SBB L		