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KIRIRI WOMEN'S UNIVERSITY OF SCIENCE AND TECHNOLOGY
UNIVERSITY EXAMINATION, 2024/2025 ACADEMIC YEAR
SECOND YEAR, SECOND SEMESTER EXAMINATION
FOR THE BACHELOR OF SCIENCE IN COMPUTER SCIENCE
KCS 304 – COMPUTER ARCHITECTURE

Date: 15TH April 2024
Time: 2:30PM – 4:30PM

INSTRUCTIONS TO CANDIDATES

ANSWER QUESTION ONE (COMPULSORY) AND ANY OTHER TWO QUESTIONS

QUESTION ONE (30 MARKS)

a) Define the following terms:
   i) Computer architecture (1 Mark)
   ii) Computer design (1 Mark)
   iii) Computer organization (1 Mark)

b) With the aid of a diagram, outline the steps taken in a basic instruction cycle during instruction processing. (5 Marks)

c) The transformation of data from main memory to cache memory is called mapping. Mapping helps to improve the performance of a computer with limited internal memory. Describe the three types of mapping in computer systems. (6 Marks)

d) The way any operand is selected during the program execution is dependent on the addressing mode of the instruction. Describe any three addressing techniques that can be employed in memory referencing. (6 Marks)

e) Highlight three differences between Complex Instruction Set Computer (CISC) and Reduced Instruction Set Computer (RISC) microprocessors. (6 Marks)

f) Jane, a 1st year student in KWUST intends to buy a computer that she could use while in the University as a tool while in the university as well in the hostels. Kindly advise her on the kind and type of a computer system he could buy. Give her the full specification of a good computer. (4 Marks)

QUESTION TWO (20 MARKS)

a) Compare and contrast SRAM and DRAM (4 Marks)

b) Highlight four differences between a hardwired and Micro-programmed control unit. (8 Marks)

c) Discuss the working of an I/O processor and how it enhances the performance of the processor. (5 Marks)

d) Calculate the average instruction processing time of a five-stage instruction pipeline for 36 instructions if conditional branch instructions occur as follows: I5, I7, I10, I25, I27. (3 Marks)

QUESTION THREE (20 MARKS)

a) Discuss the following memory access methods:
   i) Sequential access (1 Mark)
   ii) Direct access (1 Mark)
   iii) Random access (1 Mark)

b) Compare and contrast the Cache memory and the internal main memory. (6 Marks)

c) State three factors that cause instruction pipelines to deviate its normal performance. (3 Marks)

d) Using diagrams, describe the differences in programmable machines based on Von-Neumann model and the Havard Model. (8 Marks)

QUESTION FOUR (20 MARKS)

a) Explain the following memory technologies:
   i) Flash memory (1 Mark)
   ii) Virtual memory (1 Mark)
   iii) EEPROM (1 Mark)

b) Interleaved memory is a technique for compensating the relatively slow speed of Dynamic RAM. Describe the two methods for interleaving a memory. (4 Marks)

c) Discuss the memory Hierarchy on a computer system. Draw a diagram to illustrate your answer. (5 Marks)

d) Register is a very fast computer memory, used to store data/instruction in-execution. It is composed of a group of flip-flops with each flip-flop capable of storing one bit of information.
   i) Describe what is meant by a register load. (2 Marks)
   ii) State three special purpose registers and describe their roles. (6 Marks)

QUESTION FIVE (20 MARKS)

a) Using a diagram, discuss the structure and working of ALU in Computer Architecture. (6 Marks)

b) Processor chip manufacturers are increasingly developing techniques to enhance performance and reliability. Discuss three of these techniques. (6 Marks)

c) Describe four functions of ALU (4 Marks)

d) Discuss the following technologies:
   i) Smart technology (2 Marks)
   ii) Redundant Array of Independent Disks (RAID) (2 Marks)